

1. A method for estimating burn-in time for integrated circuits comprising the
2 steps of:

3 providing a substrate;

4 forming a plurality of testing structures on said substrate, each
5 substrate being formed by the steps of:

6 forming a plurality of evaluation device structures on said
7 substrate, each device structure created to permit evaluation
8 of failure mechanisms of said integrated circuit,

9 forming a first forcing input pad to provide a first forcing stimulus
10 to at least one of said evaluation device structures to provide
11 a first stimulus to stress said evaluation device structure,

12 forming a second forcing input pad to provide a second forcing
13 stimulus to at least one of said evaluation device structures
14 to further stress said evaluation device structure,

15 forming a first sensing output pad connected to sense a first
16 response from at least one of said evaluation device
17 structures,

18 forming a second sensing output pad connected to sense a
19 second response from at least one of said evaluation device
20 structures, and

21 forming a selection circuit connected to selectively communicate
22 the second stimulus to at least one selected evaluation
23 device structure and the second response from the selected
24 evaluation devices structure;
25 activating said first and second stimuli;
26 stressing said substrate;
27 examining each selected evaluation device structure for failure;
28 determining a hazard rate for each failure mechanism of said
29 integrated circuit; and
30 determining a burn-in time for said integrated circuit.

- 1 2. The method of claim 1 wherein the forming of the evaluation device
2 structure further comprises the step of:
3 stacking multiple evaluation device structures as they are formed at
4 a top surface of said substrate.
- 1 3. The method of claim 1 wherein forming the selection circuit comprises the
2 steps of:
3 forming a plurality of transmission MOS devices, each transmission
4 MOS device being connected between the first stimulus input
5 pad and one of the evaluation device structures;

6 forming a decoder circuit in communication with a gate terminal of
7 each of the plurality of transmission MOS devices to activate
8 selected transmission MOS devices to selectively connect at
9 least one of the evaluation device structures to the first stimulus
10 input pad; and

11 forming a counter circuit in communication with the decoder circuit
12 to provide an address code indicating which of the evaluation
13 device structures are to be selected.

1 4. The method of claim 3 wherein the forming the selection further comprises
2 the step of:

3 forming a function control input pad to transfer an increment signal
4 to the counter stimulating the counter to increment to modify the
5 address code to select which of the evaluation device structures
6 are selected.

1 5. The method of claim 1 wherein the evaluation device structures are
2 selected from a group of evaluation device structures consisting of
3 capacitor dielectric film evaluation devices, gate oxide integrity devices,
4 polycrystalline silicon heating devices, contact metallurgy evaluation
5 chains, interlayer via chains, MOS evaluation devices, plasma etching
6 antenna effect patterns, metal electromigration structures, memory cell
7 array, and specially designed circuit block structures.

1 6. The method of claim 1 wherein the evaluation device test structures are
2 formed in a scribe line area between the integrated circuits on said
3 substrate.

1 7. An apparatus for estimating burn-in time for integrated circuits comprising:
2 means for providing a substrate;
3 means for forming a plurality of testing structures on said substrate,
4 said means comprising:
5 means for forming a plurality of evaluation device structures on
6 said substrate, each device structure created to permit
7 evaluation of failure mechanisms of said integrated circuit,
8 means for forming a first forcing input pad to provide a first
9 forcing stimulus to at least one of said evaluation device
10 structures to provide a first stimulus to stress said evaluation
11 device structure,
12 means for forming a second forcing input pad to provide a
13 second forcing stimulus to at least one of said evaluation
14 device structures to provide a second stimulus to further
15 stress said evaluation device structure,

16 means for forming a first sensing output pad connected to sense
17 first response from at least one of said evaluation device
18 structures,

19 means for forming a second sensing output pad connected to
20 sense a second response from at least one of said
21 evaluation device structures, and

22 means for forming a selection circuit connected to selectively
23 communicate the second stimulus to at least one selected
24 evaluation device structure and the second response from
25 the selected evaluation devices structure;

26 means for activating said first and second stimuli;

27 means for stressing said substrate;

28 means for examining each selected evaluation device structure for
29 failure;

30 means for determining a hazard rate for each failure mechanism of
31 said integrated circuit; and

32 means for determining a burn-in time for said integrated circuit.

1 8. The apparatus of claim 7 wherein the means for forming of the evaluation
2 device structure further comprises:

3 means for stacking multiple evaluation device structures as they
4 are formed at a top surface of said substrate.

5 9. The apparatus of claim 7 wherein means for forming the selection circuit
6 comprises:

7 means for forming a plurality of transmission MOS devices, each
8 transmission MOS device being connected between the first
9 stimulus input pad and one of the evaluation device structures;

10 means for forming a decoder circuit in communication with a gate
11 terminal of each of the plurality of transmission MOS devices to
12 activate selected transmission MOS devices to selectively
13 connect at least one of the evaluation device structures to the
14 first stimulus input pad; and

15 means for forming a counter circuit in communication with the
16 decoder circuit to provide an address code indicating which of
17 the evaluation device structures are to be selected.

1 10. The apparatus of claim 9 wherein the means for forming the selection
2 further comprises:

3 means for forming a function control input pad to transfer an
4 increment signal to the counter stimulating the counter to

5 increment to modify the address code to select which of the
6 evaluation device structures are selected.

1 11. The apparatus of claim 7 wherein the evaluation device structures are
2 selected from a group of evaluation device structures consisting of
3 capacitor dielectric film evaluation devices, gate oxide integrity devices,
4 polycrystalline silicon heating devices, contact metallurgy evaluation
5 chains, interlayer via chains, MOS evaluation devices, plasma etching
6 antenna effect patterns, metal electromigration structures, memory cell
7 array, and specially designed circuit block structures.

1 12. The apparatus of claim 7 wherein the evaluation device test structures are
2 formed in a scribe line area between the integrated circuits on said
3 substrate

1 13. A reliability testing structure formed on a substrate comprising:
2 a plurality of evaluation device structures formed on said
3 substrate, each device structure created to permit evaluation
4 of one of a plurality of failure mechanisms of said integrated
5 circuit;
6 a first forcing input pad to provide a first forcing stimulus to at
7 least one of said evaluation device structures to provide a
8 first stimulus to stress said evaluation device structure;

9 a second forcing input pad to provide a second forcing stimulus
10 to at least one of said evaluation device structures to provide
11 a second stimulus to further stress said evaluation device
12 structure;

13 a first sensing output pad connected to sense first response
14 from at least one of said evaluation device structures;

15 a second sensing output pad connected to sense a second
16 response from at least one of said evaluation device
17 structures; and

18 a selection circuit connected to selectively communicate the
19 second stimulus to at least one selected evaluation device
20 structure and the second response from the selected
21 evaluation device structure.

- 1 14. The reliability testing structure of claim 13 wherein multiple evaluation
2 device structures are stacked as they are formed at a top surface of said
3 substrate.

- 1 15. The reliability testing structure of claim 13 wherein the selection circuit
2 comprises:

3 a plurality of transmission MOS devices, each transmission MOS
4 device being connected between the first stimulus input pad and
5 one of the evaluation device structures;

6 a decoder circuit in communication with a gate terminal of each of
7 the plurality of transmission MOS devices to activate selected
8 transmission MOS devices to selectively connect at least one of
9 the evaluation device structures to the first stimulus input pad;

10 and

11 a counter circuit in communication with the decoder circuit to create
12 from an increment signal, an address code indicating which of
13 the evaluation device structures are to be selected.

1 16. The reliability testing structure of claim 15 wherein the selection circuit
2 further comprises:

3 a function control input pad to transfer the increment signal to the
4 counter stimulating the counter to increment to modify the
5 address code to select which of the evaluation device structures
6 are selected.

1 17. The reliability testing structure of claim 15 wherein the counter circuit
2 comprises;

3 an adder circuit which sums a next address code with the
4 increment signal to generate the next address code;

5 a first transmission gate in communication with the adder circuit to
6 selectively transmit the next address code;

7 a first buffer in communication with the first transmission gate to
8 receive and retain the next address code;

9 a second transmission gate in communication with the first buffer to
10 selectively transmit the next address code from the first buffer;
11 and

12 a second buffer in communication with the second transmission
13 gate to receive, retain and then transfer to the decoder the next
14 address code.

1 18. The reliability testing structure of claim 17 further comprising

2 a clock modulator that receives the increment signal and provides
3 first and second increment signals to selectively activate the first
4 and second transmission gates to transfer the next address
5 code to the first and second buffers.

1 19. The reliability testing structure of claim 17 further comprising:

2 a first delaying circuit between the adder circuit and the first
3 transmission gate to adjust timing of the transmitting of the next
4 address code from the adder circuit to the first transmission
5 gate;

6 a second delaying circuit between the first transmission gate and
7 the first buffer to adjust timing of the transmitting of the next
8 address code from the first transmission gate to the first buffer;

9 a third delaying circuit between the first buffer and the second
10 transmission gate to adjust timing of the transmitting of the next
11 address code from the first buffer to the second transmission
12 gate; and

13 a fourth delaying circuit between the second transmission gate and
14 the second buffer to adjust timing of the transmitting of the next
15 address code from the second transmission to the second
16 buffer;

1 20. The reliability testing structure of claim 17 further comprising:

2 an initial value circuit in communication with the first buffer and the
3 second transmission gate to establish an initial value for said
4 next address code.

1 21. The reliability structure of claim 17 wherein the adder comprises:

2 a first summing circuit connected to receive and add the increment
3 signal and a least significant bit of the present address code to
4 form a least significant bit of a next address code;

5 a first carry circuit connected to receive the increment signal and
6 the least significant bit of the present address code to determine
7 a first carry bit from the sum of the increment signal and the
8 least significant bit of the present address code;

9 a plurality of summing circuits, each summing circuit connected to
10 receive and add one of plurality of bits of the present address
11 code and a carry bit determined from an adjacent less
12 significant bit of the next address code to form one of a plurality
13 of bits of the next address code; and

14 a plurality of carry circuits, each carry circuit connected to receive
15 one of the plurality of bit of the present address code and the
16 carry bit determined from the adjacent less significant bit of the
17 present address code to form one of a plurality of carry bits.

- 1 22. The reliability testing structure of claim 21 wherein the first summing circuit
2 and the plurality of summing circuits are exclusive-OR gates
- 1 23. The reliability testing structure of claim 22 wherein each exclusive-OR
2 gate comprises:

3 a MOS transistor of a first conductivity type having a gate
4 connected to a first input terminal and drain connected to a
5 second input terminal;
6
7 a MOS transistor of a second conductivity type having a gate
8 connected to a first input terminal and drain connected to a
9 second input terminal;
10
11
12 a first inverter circuit having an input connected to a source of the
13 MOS transistor of the first conductivity type and an output
14 connected to a source of the MOS transistor of the second
15 conductivity type;
16
17 a second inverter circuit having an input connected to the source of
18 the MOS transistor of the second conductivity type and an
19 output connected to the source of the MOS transistor of the first
20 conductivity type; and
21
22 an output terminal formed at the connection of the source of the
23 MOS transistor of the first conductivity type, the output of the
24 first inverter circuit, and the input of the first inverter circuit.

1 24. The reliability testing structure of claim 21 wherein the carry circuit is an
2 AND circuit.

1 25. The reliability testing structure of claim 24 wherein the AND circuit
2 comprises:

3 a first MOS transistor the first conductivity type having a gate
4 connected to a first input terminal, a source connected to an
5 output terminal, and a drain connected to a voltage reference
6 terminal;

7 a second MOS transistor of the second conductivity type a gate
8 connected to a second input terminal, a source connected to the
9 output terminal, and a drain connected to a voltage reference
10 terminal; and

11 a first depletion MOS transistor of the second conductivity type
12 having a gate and source connected to the output terminal and
13 a drain connected to a voltage supply terminal.

1 26. The reliability testing structure of claim 18 wherein the clock modulator
2 circuit comprises:

3 a resistor capacitor network connected to receive the increment
4 signal, to slow transitions of the increment signal so as to adjust
5 a time at which said increment signal is at an active voltage
6 level,

7 a first buffering circuit connected to the resistor capacitor network to
8 generate the first increment signal from the increment signal
9 with the slowed transitions; and

10 a second buffering circuit connected to the resistor capacitor
11 network to generate the second increment signal from the
12 increment signal with slowed transitions.

1 27. The reliability testing structure of claim 20 wherein the initial value circuit
2 comprises:

3 a resistor having a first terminal connected to a voltage supply
4 terminal;

5 a capacitor having a first terminal connected to a second terminal of
6 the resistor and second terminal connected to a voltage
7 reference terminal;

8 a plurality of second depletion MOS transistors of the first
9 conductivity type, each second depletion MOS transistors of the
10 first conductivity type having a gate connected to the connection
11 of the first terminal of the capacitor and the second terminal of
12 the resistor, a source connected to the voltage supply terminal
13 and a drain connected to an output of the first buffer.

1 28. The reliability testing structure of claim 13 wherein the evaluation device
2 structures are selected from a group of evaluation device structures
3 consisting of capacitor dielectric film evaluation devices, gate oxide
4 integrity devices, polycrystalline silicon heating devices, contact metallurgy
5 evaluation chains, interlayer via chains, MOS evaluation devices, plasma
6 etching antenna effect patterns, metal electromigration structures, memory
7 cell array, and specially designed circuit block structures.

1 29. The reliability testing structure of claim 13 wherein the evaluation device
2 test structures are formed in a scribe line area between the integrated
3 circuits on said substrate.

1 30. A reliability evaluation test structure to reduce area requirements of said
2 test structure when formed on a substrate, comprising:
3 a plurality of evaluation devices formed on a surface of the
4 substrate such that multiple evaluation devices are placed on
5 said substrate in a stack; and
6 at least one input/output pad connected to said evaluation devices
7 to communicate a stimulus to selected evaluation devices and
8 response from said evaluation devices.

1 31. The reliability evaluation test structure of claim 30 wherein the evaluation
2 devices are selected from a group of evaluation devices consisting of
3 capacitor dielectric film evaluation devices, gate oxide integrity devices,

4 polycrystalline silicon heating devices, contact metallurgy evaluation
5 chains, interlayer via chains, MOS evaluation devices, plasma etching
6 antenna effect patterns, metal electromigration structures, memory cell
7 array, and specially designed circuit block structures.

1 32. The reliability evaluation test structure of claim 30 wherein the reliability
2 evaluation test structure is formed in a scribe line area between the
3 integrated circuits on said substrate.

1 33. An integrated circuit wafer, comprising:

2 a substrate on to which multiple integrated circuit die are formed;
3 a plurality of evaluation devices formed on a surface of the
4 substrate such that multiple evaluation devices are placed on
5 said substrate in a stack; and
6 at least one input/output pad connected to said evaluation devices
7 to communicate stimulus to selected evaluation devices and
8 response from said evaluation devices.

1 34. The reliability evaluation test structure of claim 33 wherein the evaluation
2 devices are selected from a group of evaluation devices consisting of
3 capacitor dielectric film evaluation devices, gate oxide integrity devices,
4 polycrystalline silicon heating devices, contact metallurgy evaluation
5 chains, interlayer via chains, MOS evaluation devices, plasma etching

6 antenna effect patterns, metal electromigration structures, memory cell
7 array, and specially designed circuit block structures.

1 35. The reliability evaluation test structure of claim 33 wherein the reliability
2 evaluation test structures are formed in a scribe line area between the
3 integrated circuit die on said substrate.

1 36. A method for forming a reliability testing structure on a substrate
2 comprising the steps of:

3 providing a substrate;

4 forming a plurality of testing structures on said substrate, each
5 testing structure being formed by the steps of:

6 forming a plurality of evaluation device structures on said
7 substrate such that multiple evaluation device structures are
8 placed on said substrate in a stack, each device structure
9 created to permit evaluation of failure mechanisms of said
10 integrated circuit and ,

11 forming a first forcing input pad to provide a first forcing stimulus
12 to at least one of said evaluation device structures to provide
13 a first stimulus to stress said evaluation device structure,

14 forming a second forcing input pad to provide a second forcing
15 stimulus to at least one of said evaluation device structures

16 to provide a second stimulus to further stress said evaluation
17 device structure,

18 forming a first sensing output pad connected to sense first
19 response from at least one of said evaluation device
20 structures,

21 forming a second sensing output pad connected to sense a
22 second response from at least one of said evaluation device
23 structures, and

24 forming a selection circuit connected to selectively communicate
25 the second stimulus to at least one selected evaluation
26 device structure and the second response from the selected
27 evaluation devices structure;

1 37. The method of claim 36 wherein the evaluation devices are selected from
2 a group of evaluation devices consisting of capacitor dielectric film
3 evaluation devices, gate oxide integrity devices, polycrystalline silicon
4 heating devices, contact metallurgy evaluation chains, interlayer via
5 chains, MOS evaluation devices, plasma etching antenna effect patterns,
6 metal electromigration structures, memory cell array, and specially
7 designed circuit block structures.

1 38. The method of claim 36 wherein the reliability evaluation test structure is
2 formed in a scribe line area between integrated circuits on said substrate.